CLAIMS

1. (Currently amended) An automatic phase and frequency adjust circuit, comprising:

a phase locked loop circuit to generate a phase locked loop clock responsive to a reference signal;

an edge detector circuit to generate an edge pulse signal corresponding to a transition of an analog data signal above a predetermined threshold responsive to a pixel clock;

a phase detector circuit to generate a phase adjust signal responsive to a phase of the phase locked loop clock and the edge pulse signal; and

a phase adjust circuit to generate the pixel clock responsive to the phase adjust signal and the phase locked loop clock, where the phase adjust circuit generates a plurality of delayed clock signals by delaying the phase locked loop clock.

2. (Original) The automatic phase and frequency adjust circuit of claim 1 wherein the phase locked loop circuit comprises:

a phase detector adapted to receive the reference signal;

a loop filter coupled to the phase detector;

a voltage controlled oscillator coupled to the loop filter;

a feedback loop adapted to receive the phase locked loop clock and provide a feedback signal responsive to a frequency adjust signal.

3. (Original) The automatic phase and frequency adjust circuit of claim 1 wherein the reference signal is a horizontal synchronization signal.

4. (Canceled)

5. (Currently amended) The automatic phase and frequency adjust circuit of claim 1 [[4]] wherein the threshold is programmable.

6. (Currently amended) The automatic phase and frequency adjust circuit of claim 1 wherein the edge detector generates ~~an~~ the edge pulse corresponding to a rising, falling, or both rising and falling edges of the analog data signal.

7. (Previously presented) The automatic phase and frequency adjust circuit of claim 1 wherein the phase adjust circuit adjusts the phase of the pixel clock by delaying the reference signal.

8. (Previously presented) The automatic phase and frequency adjust circuit of claim 1 wherein the phase adjust circuit adjusts the phase of the pixel clock by delaying the phase locked loop clock.

9. (Previously presented) The automatic phase and frequency adjust circuit of claim 8 wherein the phase adjust circuit comprises:

a clock delay circuit to generate a plurality of delayed clock signals by delaying the phase locked loop clock; and

a multiplexer to select one of the plurality of delayed clock signals as the pixel clock responsive to a phase adjust signal.

10. (Original) The automatic phase and frequency adjust circuit of claim 9 wherein the clock delay circuit comprises an n-stage delay locked loop, each stage generating a corresponding delayed clock phase, each delayed clock phase being 360/n degrees out of phase.

11. (Currently amended) The automatic phase and frequency adjust circuit of claim 1 ~~wherein the phase adjust circuit generates a plurality of delayed clock signals by delaying the phase locked loop clock; and~~

wherein the phase detector comprises:

a phase hit detector to generate a plurality of phase hit enable signals corresponding to the plurality of delayed clock signals and assert one of the phase hit enable signals responsive to the edge pulse signal; and

a phase hit counter to count asserted phase hit enable signals for each of the delayed clock signals over a predetermined time.

12. (Original) The automatic phase and frequency adjust circuit of claim 11 wherein the predetermined time is a number of image scan lines.

13. (Previously presented) The automatic phase and frequency adjust circuit of claim 11 wherein the phase hit detector comprises:

a plurality of flip-flop circuits corresponding to the plurality of delayed clock signals to generate a corresponding plurality of phase out signals; and

a comparison circuit to comparing the plurality of phase out signals.

14. (Previously presented) The automatic phase and frequency adjust circuit of claim 13 wherein the comparison circuit compares adjacent phase out signals.

15. (Previously presented) The automatic phase and frequency adjust circuit of claim 11 wherein the phase hit counter comprises:

an enable signal to enable counting of asserted phase hit enable signals; and

a clear signal to clear the phase hit counter.

16. (Previously presented) The automatic phase and frequency adjust circuit of claim 11 comprising:

a phase count analysis circuit to generate phase and frequency adjust signals by analyzing the count of asserted phase hit enable signals.

17. (Previously presented) The automatic phase and frequency adjust circuit of claim 1 comprising an auto calibration circuit to align the analog data signal with the pixel clock.

18-42. (Canceled)